REMARKS

The rejection of claims 9-16 under 35 USC 102(b) as being anticipated by Novis et al (USP 4,816,726) is respectfully traversed.

Claim 9 has been amended to indicate that the first transistor is turned OFF and the second transistor is turned ON by a first brake control circuit in accordance with a brake operation instruction signal while simultaneously forcing the first transistor to be turned OFF by a second brake control signal, before the first transistor is turned OFF by the first brake control signal. Stated otherwise, claim 9, as amended, now recites that the first transistor is forced to be turned OFF by the second brake control circuit in accordance with the brake operation instruction signal before the first transistor is actually turned OFF by the first brake control circuit.

This feature is not disclosed in the Novis et al reference, nor would there be any basis for incorporating this feature in the Novis et al reference. The advantage of this feature to the subject invention is that the first transistor can be turned OFF by the second brake control circuit before the first transistor is turned OFF by the first brake control circuit, thereby more rapidly turning OFF the first transistor in a shorter time interval. This reduces the time during which both the first transistor and second transistor are ON and reduces the current flow to the ground via the first and second transistors.

Accordingly, claim 9, as amended, is clearly patentable over Novis et al and the rejection thereof should be withdrawn.

Claims 10-16 are dependent claims which are believed to be patentable over Novis et al for the same reasons as given with regard to claim 9.

The rejection of claims 1-8 under 35 USC 103(a) as unpatentable over Novis et al in view of Uchiyama et al (USP 6,072,292) is respectfully traversed.

The Uchiyama et al reference discloses two separate control system circuits that controls two motors respectively. The control system circuits may in turn be

controlled by a common signal supplied to both of the two separate control system circuits. One control system circuit has have transistors which control one of the motors whereas the other control system circuit controls the other of the two motors.

Accordingly, the two separate control system circuits do not control the same motor, much less through control of the same transistors in each of the brake control circuits.

On the other hand, the motor drive circuit of claim 1 has only one motor connected to a connection point between the first and second transistors, which are controlled by the first and second brake control circuits. That is, the motor drive circuit is defined by one control system that controls one motor connected between the first and second transistors of the first and second brake control circuits respectively.

Thus, the control system of the Uchiyama et al reference is completely different from the control system (motor drive circuit) of the present invention.

Moreover, there is no basis or motivation to combine the Uchiyama et al reference which employs two motors and two separate controls for each of the two motors with the Novis et al reference, which is directed to one control system for controlling one motor. In fact, with regard to the control of any given one motor there is no commonality between the references.

For all of the above reasons, claim 1 is clearly patentable over Novis et al taken alone or in combination with Uchiyama et al.

Claims 2-8 are dependent from claim 1 and should be patentable for the same reasons as given relative to claim 1.

New claims 17-20 are directed to a motor drive circuit similar in scope to that of claims 1-8 and require the motor to be connected to a connection point between the first and second transistors with a first brake control circuit and a second brake control circuit for turning the first transistor and the second transistor OFF and ON, based upon the brake operation instruction signal to their respective first and second brake control circuits.

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For all of the above reasons, applicant believes claims 1-20 to be clearly patentable over the art of record.

Reconsideration and allowance of claims 1-20 is respectfully solicited.

Respectfully submitted,

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MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on <u>June 9, 2005</u>.

Date: June 9, 2005